Claim Amendments

Claims 1-45 (Previously canceled).

46. (Previously presented) A method of fabricating complementary high-voltage field-effect transistors (HVFETs) in a substrate of a first conductivity type comprising:

forming first and second well regions of a second conductivity type in the substrate;

forming a first source region in the substrate adjacent the first well region;

forming a first drain region of the second conductivity type in the first well region;

forming second and third drain regions of the first conductivity type in the second well region, the second drain region being separated from the third drain region;

forming a second source region of the first conductivity type in the second well region, the second source region being separated from the second drain region;

forming first and second buried layers within the first and second well regions, respectively, the second buried layer being connected to the second and third drain regions; and

forming first and second insulated gates.

47. (Previously presented) The method of claim 46 wherein the first insulated gate is formed above an area of the substrate that separates the first source region from the first well region.

48. (Previously presented) The method of claim 47 wherein the second insulated gate is formed above an area of the second well region that separates the second source region from the second drain region.

49. (Previously presented) The method of claim 46 wherein the first conductivity type is P-type and the second conductivity type is N-type.

50. (Previously canceled).

51. (Previously presented) A method of fabricating complementary power transistors in a substrate of a first conductivity type comprising:

forming first and second well regions of a second conductivity type opposite to the first conductivity type in the substrate;

forming first and second drain regions of the first conductivity type in the first well region, the second drain region being separated from the first drain region;

forming a third drain region of the second conductivity type in the second well region;

forming first and second buried layers within the first and second well regions, respectively, the first buried layer adjoining the first and second drain regions; and

forming first and second insulated gates.

52. (Previously presented) The method according to claim 51 wherein the first conductivity type is P-type.

53. (Previously presented) The method according to claim 51 wherein the first and second buried layers are formed simultaneously by implanting a first dopant.

54. (Previously presented) The method according to claim 53 wherein the dopant is boron.

Claims 55-59 (Previously canceled).